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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/831,241	05/03/2001	Simon Pearce	R&G C-321	4577
7590	03/01/2004		EXAMINER	
Flynn Thiel Boutell & Tanis 2026 Rambling Road Kalamazoo, MI 49008-1699			CASCHERA, ANTONIO A	
			ART UNIT	PAPER NUMBER
			2676	11
DATE MAILED: 03/01/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/831,241	PEARCE, SIMON	
	Examiner	Art Unit	
	Antonio A Caschera	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 22 December 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) 1,2,5 and 7 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 3,4,8-11,14-16 and 21-23 is/are rejected.
- 7) Claim(s) 6,12,13,17-20 and 24 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 03 May 2001 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in the pending application.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3, 4, 6 and 10-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claims 10 and 14 do not particularly point out and distinctly claim the subject matter which the applicant regards as the invention as the newly amended claims fail to specify which particular type of, "mip-map data," (compressed or decompressed) is utilized in the "lower-level mip-map generator." For example, in claim 10, in the section pertaining to the "lower-level mip-map generator," the claim recites, "lower-level mip-map generator means coupled to said cache means for receiving the mip-map data..." (see lines 22-24 of claim 10). The office is unsure as to which mip-map data, either the compressed or decompressed, the applicant is referring to. The office, therefore, suggests adding the identifier of, "decompressed" or "compressed" into the above claim language in order to clarify and particularly point out the

claim limitations. The same rationale can be applied to the, "generating" of mip-map data section in claim 14.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 8 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Tarolli et al. (U.S. Patent 5,822,452).

In reference to claims 8 and 9, Tarolli et al. discloses a method and apparatus for compressing texture images, storing compressed images and decompressing texture images (see column 3, lines 51-54). Tarolli et al. discloses representing texture data by compressed codes (see column 7, lines 6-8 and Figure 7). Tarolli et al. also discloses converting each texture in a texture image to a selected color space using a decompression code table (see column 4, lines 15-17 and Figure 7). Tarolli et al., for example, discloses converting texels from RGB to YAB color space using equations which the office interprets as substantially similar to taking weight averages of the RGB components to calculate a converted space component (see column 8, lines 1-8). These components are then stored in a decompression code table (see #502, 504, 514 and 516 of Figure 5 and Figures 6A-7). Note, the office believes Tarolli et al. therefore inherently discloses other colors based upon principal colors in the RGB color space as principal colors,

red, green and blue can be manipulated to produce other colors. Tarolli et al. discloses interpolating means in the form of a blending unit which produces an output pixel value, representing an output texel, from input texels (see column 6, lines 46-52). Tarolli et al. further discloses that when a texture image is requested, the decompression table is selected from RAM and is stored and utilized in each decompression unit (see #320a-d of Figure 3) which passes its output to a blending unit which produces a pixel value representative of texel data (see column 17, lines 19-30, 44-51 and Figure 4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schilling et al. (U.S. Patent 6,236,405 B1) in view of Hannah et al. (U.S. Patent 5,548,709).

In reference to claims 10 and 14, Schilling et al. discloses a three-dimensional graphics system incorporating texture mapping methods (see column 2, lines 7-9 and column 4, lines 27-29). Schilling et al. also discloses a memory means for storing mip-map data for use in texturing an image, the mip-map data made up of levels of decreasing resolution (see column 4, lines 9-23 and Figure 2). Schilling et al. discloses a compression/decompression means for compressing/decompressing texture data stored in memory (see columns 5-6, lines 45-13). Schilling et al. discloses a cache, coupled to a DRAM controller, which stores color data, which

in the present invention represents the texture data, retrieved from memory (see column 7, lines 37-44 and #614 of Figure 6). Schilling et al. discloses retrieving compressed texels from memory and decompressing the texel data (see column 6, lines 2-5). Schilling et al. discloses bilinear interpolation performed on four neighboring texel colors in accordance with the pixel center coordinates (see column 7, lines 49-55). Schilling et al. discloses the interpolator coupled to receive data from the cache via a color extraction unit and output data to a rasterizer (see #607, 614, 618 and 622 of Figure 6). Schilling et al. also discloses a modified embodiment of the invention where a complete trilinear interpolation is performed instead of bilinear interpolation (see column 7, lines 56-60). Schilling et al. does not explicitly disclose an input means for receiving input data indicating the type of mip-map data required and the level of the mip-map however Hannah et al. does. Hannah et al. discloses an apparatus and method for performing texture mapping (see lines 1-2 of abstract). Hannah et al. discloses an input/address data line communicating to a mip-map generator and memory controller, both of a TRAM (texture random access memory) (see column 5, lines 4-7 and #201-203 of Figure 2). Note, the office interprets the input data and address information received by the TRAM of Hannah et al. to provide substantially similar information as the input means input data of applicant's invention. Further note, the office interprets the memory controller of Hannah et al. to inherently retrieve texture data from memory based on the above input address information. Hannah et al. also discloses the mip-map generator producing texels for the next rougher mip-map level of the mip-map loaded from DRAM memory (see column 7, lines 9-11, 17-18, 21-31 and #202 of Figure 2). Note, the office interprets the DRAM memory substantially similar in functionally to the cache of applicant's claims. Hannah et al. also discloses an alternate embodiment

specifically using trilinear interpolation, interpolating the multi-level maps to obtain an output texel (see column 2, lines 8-15, column 8, lines 25-32, column 9, lines 10-20, 30-38 and #209 of Figure 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the mip-map generation/texture system controlling techniques of Hannah et al. with the three-dimensional texture mapping system of Schilling et al. in order to produce a faster, more accurate and efficient texture mapping process in a computer graphics system (see column 2, lines 30-32 of Hannah et al.).

5. Claims 3, 4, 11, 15, 16 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schilling et al. (U.S. Patent 6,236,405 B1) in view of Hannah et al. (U.S. Patent 5,548,709) and further in view of Tarolli et al. (U.S. Patent 5,822,452).

In reference to claim 3, Schilling et al. and Hannah et al. disclose all of the claim limitations as applied to claim 10 above, Schilling et al. discloses retrieving compressed texels from memory and decompressing the texel data (see column 6, lines 2-5). Note, the office interprets the memory of Schilling et al. to be substantially similar in functionality to the cache of applicant's claim. Neither, Schilling et al. nor Hannah et al. explicitly disclose trilinear interpolator means directly coupled to the output of the decompression means. Tarolli et al. discloses a system and method for compressing and decompressing a texture image whereby the texture mapping system comprises decompression units coupled to a bilinear blending unit used to combine texel values (see lines 1-2 of abstract, column 6, lines 42-52 and #320a-d, 322 of Figure 3). Note, the office interprets the blending unit of Tarolli et al. substantially similar in functionality to the interpolator of applicant's claim. Tarolli et al. does not explicitly disclose utilizing trilinear interpolator means however such a limitation has been described above in

reference to claims 10, Schilling et al. and Hannah et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the decompression/interpolation connectivity and techniques of Tarolli et al. with the mip-map generation/texture system controlling techniques and three-dimensional texture mapping system of Schilling et al. and Hannah et al. in order to create a more efficient texturing system utilizing decompressed texels without performing complex multiplications (see column 3, lines 26-36 of Tarolli et al.) thereby conserving processing cycles.

In reference to claim 4, Schilling et al. and Hannah et al. disclose all of the claim limitations as applied to claim 10 above. Neither Schilling et al. nor Hannah et al. explicitly disclose cache means coupled to decompression means arranged in parallel however Tarolli et al. does. Tarolli et al. discloses four decompression units arranged in parallel connected to a texture memory (see #212c and 320a-d of Figure 3). Tarolli et al. does not explicitly disclose four caches arranged in parallel however, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement four separate memory units instead of the single texture memory of Tarolli et al. Applicant has not disclosed that utilizing specifically four caches provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the single texture memory unit of Tarolli et al. especially because Tarolli et al. discloses a texture memory addresser able to request specific texels from the texture memory (see column 6, lines 37-42 and #308 of Figure 3) and even further because the office interprets the particular design using four separate caches to be a matter of design choice as preferred by the designer or to which best suits the application at hand. Therefore, it would have been obvious

to one of ordinary skill in this art to modify Schilling et al., Hannah et al. and Tarolli et al. to obtain the invention as specified in claim 4. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the decompression/interpolation connectivity and techniques of Tarolli et al. with the mip-map generation/texture system controlling techniques and three-dimensional texture mapping system of Schilling et al. and Hannah et al. in order to create a more efficient texturing system utilizing decompressed texels without performing complex multiplications (see column 3, lines 26-36 of Tarolli et al.) thereby conserving processing cycles.

In reference to claim 11, Schilling et al. and Hannah et al. disclose all of the claim limitations as applied to claim 4 above. Claim 11 is similar in scope to claim 5 and therefore is rejected under similar rationale even further however, Tarolli et al. also discloses each decompression unit receiving a signal from a control register identifying which decompression table is associated with an 8-bit compressed value for each texel (see column 18, lines 28-31). Note the office interprets the control register substantially similar in functionality to a “first allocating means” of applicant’s claim. Neither Schilling et al., Hannah et al. nor Tarolli et al. explicitly disclose four cache means however, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement four separate memory units instead of the single texture memory of Tarolli et al. Applicant has not disclosed that utilizing specifically four caches provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant’s invention to perform equally well with the single texture memory unit of Tarolli et al. especially because Tarolli et al. discloses a texture memory addresser able to request specific texels from

the texture memory (see column 6, lines 37-42 and #308 of Figure 3) and even further because the office interprets the particular design using four separate caches to be a matter of design choice as preferred by the designer or to which best suits the application at hand. Therefore, it would have been obvious to one of ordinary skill in this art to modify Schilling et al., Hannah et al. and Tarolli et al. to obtain the invention as specified in claim 11.

In reference to claims 15 and 16, Schilling et al. and Hannah et al. disclose all of the claim limitations as applied to claim 11 above. Tarolli et al. discloses four decompression units receiving compressed data from a texture memory supplying one texel each to a blending unit (see column 6, lines 42-52, #212C, 320a-d of Figure 3, #502, 504, 514, 516 of Figure 5 and Figure 7). Note, the term “a maximum” in reference to the first and second decompression means of applicant’s claim is broadly interpreted as the range of values 0-4 and 0-2, respectively for the first and second decompression means of applicant’s claim, therefore Tarolli et al. overcomes such a limitation. Note, the office interprets Tarolli et al. to inherently disclose means substantially similar to the “selecting upper texel means” of applicant’s claim as the texels output from the decompression units of Tarolli et al. are forwarded to a blending unit for interpolation means (see column 6, lines 48-52). Further, in reference to claim 16, Tarolli et al. discloses the decompression units to each calculate an RGB representative texel value and therefore select or define texels (see column 20, lines 19-25 and Figure 10). Again, Tarolli et al. does not explicitly disclose four caches arranged in parallel however, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement four separate memory units instead of the single texture memory of Tarolli et al. Applicant has not disclosed that utilizing specifically four caches provides an advantage, is used for a particular

purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the single texture memory unit of Tarolli et al. especially because Tarolli et al. discloses a texture memory addresser able to request specific texels from the texture memory (see column 6, lines 37-42 and #308 of Figure 3) and even further because the office interprets the particular design using four separate caches to be a matter of design choice as preferred by the designer or to which best suits the application at hand. Therefore, it would have been obvious to one of ordinary skill in this art to modify Schilling et al., Hannah et al. and Tarolli et al. to obtain the invention as specified in claim 15.

In reference to claim 21, Schilling et al. and Hannah et al. disclose all of the claim limitations as applied to claim 14 above. Hannah et al. also discloses the mip-map generator producing texels for the next rougher mip-map level of the mip-map loaded from DRAM memory (see column 7, lines 9-11, 17-18, 21-31 and #202 of Figure 2). Tarolli et al. discloses four decompression units receiving compressed data from a texture memory supplying one texel each to a blending unit (see column 6, lines 42-52, #212C, 320a-d of Figure 3, #502, 504, 514, 516 of Figure 5 and Figure 7). Note, the office interprets the texture memory substantially similar to the cache memory of applicant's claim. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the mip-map generator of Hannah et al. with the decompression units of Tarolli et al. in order to operate on decompressed data rather than compressed data as one of the main reasons for compression is to preserve memory space when saving data.

In reference to claims 22 and 23, Schilling et al. and Hannah et al. disclose all of the claim limitations as applied to claim 14 above. Tarolli et al. discloses four decompression units

receiving compressed data from a texture memory supplying one texel each to a blending unit (see column 6, lines 42-52, #212C, 320a-d of Figure 3, #502, 504, 514, 516 of Figure 5 and Figure 7). Again, Tarolli et al. does not explicitly disclose four caches storing the compressed data however, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement four separate memory units instead of the single texture memory of Tarolli et al. Applicant has not disclosed that utilizing specifically four caches provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the single texture memory unit of Tarolli et al. especially because Tarolli et al. discloses a texture memory addresser able to request specific texels from the texture memory (see column 6, lines 37-42 and #308 of Figure 3) and even further because the office interprets the particular design using four separate caches to be a matter of design choice as preferred by the designer or to which best suits the application at hand. Therefore, it would have been obvious to one of ordinary skill in this art to modify Schilling et al., Hannah et al. and Tarolli et al. to obtain the invention as specified in claims 22 and 23.

Response to Arguments

5. The office notes the cancellation of claims 1, 2, 5 and 7 along with the addition of claims 15-24.

6. Applicant's arguments, see page 15, 4th paragraph, filed 12/22/2003, with respect to the disclosure have been fully considered and are persuasive. The objection of the disclosure has

been withdrawn since minor informalities have been corrected. Note, the abstract has been considered and is accepted.

7. Applicant's arguments, see page 15, 4th paragraph, filed 12/22/2003, with respect to the drawings have been fully considered and are persuasive. The objection of the drawings has been withdrawn since minor informalities have been corrected.

8. Applicant's arguments with respect to claims 3, 8, 9, 10, 13 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

9. Claims 6, 12, 13, 17-20 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In reference to claims 6, 12, 13 and 24, the prior art of record (Schilling et al., Hannah et al. and Tarolli et al.) does not explicitly disclose the lower-level mip-map generator comprising four interpolators operating upon sixteen texels providing an output of four texels for the next below mip-map in combination with the further limitations of claims 6, 12 and 13.

In reference to claims 17 and 19, the prior art of record (Schilling et al., Hannah et al. and Tarolli et al.) does not explicitly disclose four filtering means producing a texel for the next below level of a mip-map by filtering in compressed form in combination with the further limitations of claims 17 and 19.

In reference to claim 18 and 20, claims 18 and 20 depend upon objected claims 17 and 19 respectively and are therefore also objected.

References Cited

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- a. Migdal et al. (U.S. Patent 5,760,783)
 - Migdal et al. discloses an apparatus and method for quickly and efficiently providing texel data relevant for displaying a textured image.
- b. Walton (U.S. Patent 6,154,216)
 - Walton discloses a method and apparatus for decompression of a two dimensional video texture map.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Antonio Caschera whose telephone number is (703) 305-1391. The examiner can normally be reached Monday-Thursday and alternate Fridays between 7:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella, can be reached at (703)-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

aac

2/24/04

Matthew C. Bella

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